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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,898	07/31/2003	Bar-Chung Hwang	Q76735	9624

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EXAMINER	
BATAILLE, PIERRE MICHE	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/630,898	HWANG ET AL.	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The present Office Action is taken in response to applicant's communication filed March 6, 2006 responding to Office Rejection dated December 6, 2006. Applicant's amendments and/or arguments have been considered with the results that follow. Claims 1 and 2-20 are now pending in the application under prosecution as claim 2 has been canceled by applicant's amendment. No new claims have been added

Response to Arguments

2. Applicant's arguments filed March 6, 2006 with respect to claims 1 and 3-20 have been fully considered but they are not persuasive for at least the following remarks.

Applicant contend that the Mick's reference discloses two devices 205 and 206 to share a memory device 201, which is different from applicant claimed invention that provides a device to access a plurality of memory locations. However, the fact that the two devices share a memory device does not remove the reference from reading upon the claims. The arbitration feature, as clearly indicated by the application is the actual proof of sharing of more than one port as "a port coupling circuitry selectively couples selected memory banks to the left and right ports in response to the bank access grant signals. Mick discloses left and right memory bank address circuits having left and right status registers storing value of the right and left memory banks and in responding to access a port coupling circuitry selectively couples selected memory banks to the left and right ports in response to the bank access grant signals.

FIG. 3 of Mick's reference features an illustration of a block diagram of a portion of the memory device 201 including memory banks (which applicant noted as a single device) and port coupling logic and a semaphore logic circuit providing control signals in the form of left and right-side bank access grant signals. Clearly a plurality of memory locations, as claimed by the applicant, correspond to plurality of memory banks as, illustrated in Fig. 3 of Mick.

Mick clearly teaches a status register having at least one bit indicative of a written status of at least one mailbox register associated with the fist port and the second port and readable to the first port and the second port. Fig. 4 of Mick's disclosure features the access requesting device being granted memory bank access of the memory device and selectively coupling circuitry selectively coupling individual ones of memory to the left and right ports. ***[Col. 2, Lines 29-31, Lines 38-41].***

Mick is believed to added al features according to claims 1 and 3-20. In view of the above remarks, the office rejection is maintained and repeated below.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,751,638 (Mick et al).

With respect to claims 1, 6, 9, 12, 15, and 18, Mick discloses a dual port structure ***(Fig. 3 and 23-24)***, wherein said structure has a first port and a second port, and a CPU ***(corresponding access requesting device Col. 5, Line 63 to Col. 6, Line 11)*** uses said dual ports structure to access said first port or said second port ***[first and second ports (left and right ports) for communicating respectively with first and second resource sharing electronic devices]***, said dual ports structure comprising: a first register bank for storing values of said first port, wherein said values comprise a first status value; a second register bank for storing values of said second port, wherein said values comprise a second status value ***(left and right memory bank address circuits having left and right status registers storing value of the right and left memory banks) [Col. 2, Lines 18-31; Col. 6, Lines 25-59; Col. 5, Lines 16-61]***; a global register for storing a control value and a mapped said first status value or mapped said second status value, or storing a control value, a mapped said first status value and mapped said second status value ***(semaphore logic control circuit 302 coupled to left and right register decoder circuits, 303 and 304, for providing addresses corresponding to register banks in the memory device 201 to generate enable signals for the registers) [Col. 2, Lines 18-31; Col. 6, Lines 25-59; Col. 5, Lines 16-61; Col. 7, Lines 1-17]***; an address decoder coupling with said CPU to decode an address signal ***(left and right register decoder 303 and 304 for decoding***

addresses); and a selector for selecting said first register bank or said second register bank to couple with said address decoder according to said control value stored in said global register, wherein said CPU can access said first register bank or said second register bank through said address decoder ***(selector/multiplexer for selectively activate left or right bank decoder circuit in response to left and right multiplexer select signal) [Col. 2, Lines 18-31; Col. 7, Lines 1-17, Fig. 16-17]***.

With respect to claims 2-5, 7-8, 10-11, 13-14, 17, and 19-20, Mick discloses the dual ports structure wherein said values comprises a status value; said first register bank and said second register bank have a same address; said second status value of said second register bank is mapped to said global register when said first register bank is coupled with said address decoder; said first status value of said first register bank is mapped to said global register when said second register bank is coupled with said address decoder ***[Col. 2, Lines 18-31; Col. 6, Lines 25-59; Col. 5, Lines 16-61; Col. 7, Lines 1-17]***.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (571) 272-4178. The examiner can normally be reached on Mon-Fri (8:00A to 4:30P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pierre-Michel Bataille
Primary Examiner
Art Unit 2186

April 30, 2006

PIERRE BATAILLE
PRIMARY EXAMINER